REMARKS

Reconsideration of the present application, as amended, is respectfully requested. Claims 1-6 are pending. Claims 1 and 5 have been amended. No claims have been cancelled or added.

The specification is objected to for containing a non-descriptive title. The title has been amended to accurately reflect the invention to which the claims are directed. As such, Applicant respectfully requests withdrawal of the objection to the title.

Claims 1-6 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,495,588 to Gibart et al. ("Gibart"). Gibart is directed to the coordination of a high-speed processor with a microprocessor that share information through the use of address and data lines and common memory components. The processor of Gibart is described as a specialized processor that runs a subset of the instructions of a general purpose microprocessor.

Independent claim 1 has been amended to include the feature that the second processor is operable to access a predetermined, non zero, selection of the registers of the first processor. In particular, independent claim 1 has been amended to include that "the first processor means includes a plurality of registers, and the second processor means is operable to access a predetermined, non-zero, selection of the said registers." Support for this amendment is found on at least page 3, lines 15-17 and page 6, lines 18-23 of the specification. Applicants respectfully submit that Gibart fails to teach at least this feature of independent claim 1. In particular, Applicants submit that Gibart does not disclose accessibility of the registers of a first processor by a second processor.

Independent claim 5 as amended is describes "a method of operating a computer including first processor means which operates to process instructions from a first set of instructions, and second processor means which operates to process instructions from a second set of instructions." The claim as amended describes the second processor receiving and processing instructions characterized in that "the first processor means includes a plurality of registers, and the second processor means is operable to access a predetermined, non-zero, selection of the said registers." Applicants respectfully submit that Gibart fails to teach at least this feature of independent claim 5. As described with respect to independent claim 1,

Applicants submit that Gibart does not disclose the ability of a second processor to access the registers of a first processor.
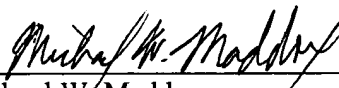
Applicants respectfully submit that amended claims 1 and 5, and those claims dependent therefrom, distinguish over Gibart. Therefore, withdrawal of the 102(b) rejection of claims 1 -6 is respectfully requested.

Claims 2-4 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gibart in view of U.S. Patent No. 5,614,847 to Kawahara et al. ("Kawahara"). Claims 2-4 are dependent upon claim 1, and claim 6 is dependent upon claim 5. Claims 2-4 and 6 distinguish over Gibart for the same reasons as stated above for amended claims 1 and 5. Kawahara is directed to a semiconductor integrated circuit and includes a capability for decreasing power consumption by using active and inactive states of operation. Applicant respectfully submits that Kawahara does not remedy the deficiency of Gibart as Kawahara does not teach the ability of a second processor to access the registers of a first processor. Therefore, Applicant respectfully submits that claims 2-4 and 6 distinguish over the combination of Gibart and Kawahara and respectfully requests the withdrawal of the 103(a) rejection.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: November 16, 2004   Respectfully submitted,

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